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LEE & HAYES, PLLC
421 W. RIVERSIDE AVE, STE 500
SPOKANE, WA 99201

| EXAMINER | |
|---|---|
| CHANG, EDITH M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2637 | |

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/891,578 | KIM ET AL. | |
| | Examiner | Art Unit | |
| | Edith M Chang | 2637 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08292001,03202002,09222003.*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: in page 15 line 1, "CLAIMS" should be changed to "I (or we claim)", "The invention claimed is" (or the equivalent), refer to MPEP 608.019(m).

Appropriate correction is required.

### *Claim Objections*

2. Claims 2-3, 5, 6-10, 13-14, 18-33 and 41-47 are objected to because of the following informalities:

Claim 2, line 2: "PVT" is suggested changing to "PVT (process, voltage, and temperature)"; and line 3: "detected a" is suggested changing to "detected".

Claim 3, lines 7-8: "produce a captured data signal" is suggested changing to "produce the captured data signal".

Claim 5, line 5: "the second control" is suggested changing to "the second digital control".

Claim 6, line 7: "clock signal;" is suggested changing to "clock signal; and"; line 8: "phase detection logic" is suggested changing to "a phase detection logic".

Claim 7, line 1: "PVT" is suggested changing to "PVT (process, voltage, and temperature)".

Claim 8, line 2: "calibration logic" is suggested changing to "a calibration logic"; and line 6: "latching logic" is suggested changing to "a latching logic".

Claims 9 & 10, line 2: "calibration logic" is suggested changing to "a calibration logic".

Claim 13, line 4: "calibration logic" is suggested changing to "a calibration logic"; line 6: "phase;" is suggested changing to "phase; and"; and line 7: "evaluation logic" is suggested changing to "an evaluation logic".

Claim 18, line 5: "calibration logic" is suggested changing to "a calibration logic"; and line 7: "signals;" is suggested changing to "signals; and".

Claim 21, line 5: "PVT" is suggested changing to "PVT (process, voltage, and temperature)", line 8: "signal;" is suggested changing to "signal; and"; and line 10: "for PVT" is suggested changing to "for the PVT".

Claim 23, line 2: "that generate" is suggested changing to "that generates"; line 5: "PVT" is suggested changing to "PVT (process, voltage, and temperature); line 6: "calibration logic" is suggested changing to "a calibration logic"; line 8: "signal;" is suggested changing to "signal; and"; and line 10: "for PVT" is suggested changing to "for the PVT".

Claim 24, line 1: "recited in claim 21" is suggested changing to "recited in claim 23".

Claim 25, line 4: "a input" is suggested changing to "an input".

Claim 41, line 9: "evaluation" is suggested changing to "an evaluation"; and line 12: "latching" is suggested changing to "a latching".

Claims 14, 19-20, 22, 26-33 and 42-47 are directly dependent on the objected claims 13, 18, 21, 25 and 41.

Appropriate corrections are required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In claim 5 lines 7-12, claim 10 lines 6-11, the phase detection logic derives at least one correction value with which the calibration logic compensates one of the two digital control values, however in the disclosure of the application, there is no drawing or description to teach the derived correction value from the phase detection logic fed back to the calibration logic for compensating one of the control values to account for different propagation delays of the first and second clock signals.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 23 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23, lines 4-5: "one or more delay elements configured to delay the measurement clock signal by a phase delay that varies with PVT variations" is not understood that how the delay elements delay the clock signal by a phase varying with PVT variations, wherein there is

no connection between the delay elements and PVT variations compensated by the PVT-sensitive circuit taught in the disclosure of the application.

Claim 24 is directly dependent on the rejected claim 23.

### *Claim Rejections - 35 USC § 102*

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 15-20 are rejected under 35 U.S.C. 102(a) as being anticipated by admitted prior art (Admission, Fig.2).

Regarding **claims 15 & 18**, in Fig.2, the Admission discloses a plurality of clock generators, elements 20 & 22 with PHASE1 setting to generate the CLK1 with phase having set PHASE1 value and elements 20 & 23 with PHASE2 setting to generate the CLK2 with phase having set PHASE2 value, wherein CLK1 is delayed by element 31 to produce phase difference; the element 22 with PHASE1 setting to vary the phase value of the CLK1 to a derived value from the new PHASE1 setting to produce a phase relationship between signals.

Regarding **claims 16 & 19**, the Admission discloses the clock signals having approximately identical phases when choosing the phase relationship by setting/deriving the control value.

Regarding **claims 17 & 20**, the Admission discloses one common reference clock.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 3-4, 6, 8-9, 11-14 and 25-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Admission, Fig.2) in view of Waters (US 5,479,457).

Regarding **claims 1 & 6**, in the Fig.2 the Prior Art, the Admission discloses a device comprising a first clock generator (element 23 with PHASE2 setting) taking in PHASE2 value to generate a clock signal with the phase of PHASE2, a second clock generator (element 22 with PHASE1 setting to generate a clock signal with the phase of PHASE1); and a phase detector (element 31) comparing the PHASE1 of the second clock signal and PHASE2 of the first clock signal, however the Admission does not specify the detail of the phase detection logic. Waters teaches the digital phase detector element 40 in Figure 4, wherein it takes two digital words from lines 48 and 50 representing the phase values of two clock signals (clock signals on lines 46 and 62) to compare and produce a phase difference on line 56. It is well known that the phase detector having the logic to compare the phases of the signals inputted, as the Admission (Fig.2) having the phase detector, it would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the phase detection logic taught by Water implemented in the element 31 of the Admission to compare the phase values to detect a phase relationship between two clock signals for the purpose of having a phase detector in the digital apparatus to minimize the digital clock jitter (column 1 lines 44-48, column 2 lines 37-45).

Regarding **claims 3 & 8**, in Fig.2, the Admission discloses the calibration logic element 22 with PHASE1 setting to set the first clock signal (CLK1) having the phase of PHASE1 value; the flip/flop element 25 clocked by the CLK1 to latch the DATAIN to produce the captured data CDATA; and elements 26 and 27 latching CDATA to produce the synchronized data signal SDATA in response to the signal on line 30 from the phase detection element 31, therefore the Admission discloses the invention recited in the claims.

Regarding **claims 4 & 9**, the Admission discloses receiving the received signal DATAIN as an oscillating signal having a clock period (as a third clock signal), the PHASE1 set to calibrate the phase if CLK1 relative to DATAIN the third clock signal; the phase detection circuit element 31 comparing the CLK1 and CLK2 to clock/determine the DATAIN.

Regarding **claims 11 & 13**, in Fig.2, the Admission discloses a clock signal CLK1 generated with a phase of the phase control value PHASE1 related to the reference clock 20; the element 22 with the PHASE1 setting varies the phase value of the clock signal CLK1 to produce a phase relationship between the CLK1 and the phase of the received signal latched at element 25, wherein the received signal can be an oscillating signal having a clock period (as a clock signal); and a phase detection circuit element 31, but the Admission does not specify the logic to evaluate the phase values. However Waters teaches the digital phase detector element 40 in Figure 4, wherein it takes two digital words from lines 48 and 50 representing the phase values of two clock signals (clock signals on lines 46 and 62) to compare and produce a phase difference on line 56. It is well known that the phase detector having the logic to compare the phases of the signals inputted, as the Admission (Fig.2) having the phase detector, it would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the

phase detection logic taught by Water implemented in the element 31 of the Admission to compare the phase values to detect a phase relationship between two clock signals for the purpose of having a phase detector in the digital apparatus to minimize the digital clock jitter (column 1 lines 44-48, column 2 lines 37-45).

Regarding **claims 12 & 14**, the Admission discloses setting PHASE1 such that the CLK1 having a phase relationship related to the phase of the DATAIN, and the relationship can be approximately equal to as choice.

Regarding **claims 25, 34 & 41**, in Fig.2, the Admission discloses a device and its method, the device comprises a clock generator generating the CLK1 with the setting PHASE1 value related to the reference source element 20, the target clock signal CLK2, and the received signal DATAIN that the CLK1 clocks the DATAIN in latch 25 to produce the captured data CDATA; the phase detection circuit element 31 to evaluate and compare the phase values of the two clock signals CLK1 and CLK2 to produce a signal on line 30 to clock the CDATA latched at 26 to produce a synchronized data clocked by CLK2, but the Admission does not specify the logic to evaluate the phase values. Waters teaches the digital phase detector element 40 in Figure 4, wherein it takes two digital words from lines 48 and 50 representing the phase values of two clock signals (clock signals on lines 46 and 62) to compare and produce a phase difference on line 56. It is well known that the phase detector having the logic to compare the phases of the signals inputted, as the Admission (Fig.2) having the phase detector, it would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the phase detection logic taught by Water implemented in the element 31 of the Admission to compare the phase values to detect a phase relationship between two clock signals for the purpose of having a phase

detector in the digital apparatus to minimize the digital clock jitter (column 1 lines 44-48, column 2 lines 37-45).

Regarding **claims 26-27 & 35-36, 43-44**, in Fig.2, the Admission discloses the phase detection circuit element 31 comparing the PHASE1 of CLK1 to a reference value represents a 90 degree phase offset/lead from the CLK2 (elements 33 & 31), wherein the element 33 delays the CLK1 comparing to CLK2.

Regarding **claims 28-30 & 40, 42**, the Admission discloses the phase detection circuit element 31 comparing the PHASE1 of CLK1 (the input phase of the input timing signal) to PHASE2 of CLK2 (the target phase of the target timing signal), wherein the CLK2 is generated in response of the set PHASE2 and CLK1 is generated in response of the set PHASE1.

Regarding **claims 31, 37 & 45**, the modified Admission device or method with Waters' teaching discloses that the phase value is a digital word on line 50 in Figure 4 of Waters '457.

Regarding **claims 32, 38 & 46**, in Fig.2 and page 3 lines 6-12 of the current application, the Admission teaches the element 31 determines the timing phase to clock the CDATA, the timing phase to be the CLK2 (choosing the element 26a) if CLK2 lags CLK1 more than 90 degree, to be the complement of CLK2 (180 degree relative to the CLK2, choosing the element 26b) if CLK2 lags CLK1 less than 90 degree.

Regarding **claims 33, 39 & 47**, in Fig.2, the Admission teaches the latch element 24 clocking the synchronized data signal SDATA with CLK2 the target timing signal.

11. Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Admission, Fig.2) in view of Waters (US 5,479,457) as applied to claims 1 and 6 above, and further in view of Brandt (US 5,859,550).

Regarding **claims 2 & 7**, the modified Admission with Water's teaching does not show the process, voltage, and temperature (PVT) circuit, however further Brandt teaches the PVT-compensated circuit in the clock distribution system in FIG.4. It would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the PVT-sensitive circuit taught by Brandt in the device that the PVT takes the CLK1 and CLK2 as inputs in response to the phase difference of the two clock signals to compensate the process, voltage, and temperature variation for the purpose to reduce the clock skew and get accurate clock signals (column 4 lines 20-25).

12. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Admission, Fig.2) in view of Brandt (US 5,859,550).

Regarding **claims 21 & 23**, in Fig.2, the Admission discloses a device and its method, the device comprising the element 22 with PHASE1 setting to generate CLK1 clock signal having phase PHASE1 set relative to the reference clock source 20; a delay element 33 delaying the CLK1 wherein the delay element is subject to PVT variation, but does not specify the PVT adjustment. However Brandt teaches the PVT-compensated circuit in the clock distribution system in FIG.4. It would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the PVT-sensitive circuit taught by Brandt

in the Admission's device that the PVT takes the delayed CLK1 from the output of element 33 and CLK2 as inputs in response to the phase difference of the two clock signals to compensate the process, voltage, and temperature variations for the purpose to reduce the clock skew and get accurate clock signals (column 4 lines 20-25). This modified device has the PVT circuit being responsive to the PVT adjustment value which is the output of the element 510 Phase Detector FIG.5 '550 to compensate the variations.

Regarding **claims 22 & 24**, the Admission teaches setting PHASE1 such that the CLK1 having a phase relationship related to the phase of the clock source 20, and the relationship being approximately equal to as choice.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
October 14, 2004

YOUNG T. TSE
PRIMARY EXAMINER